said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

22. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said wiring substrate having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

23. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said wiring substrate having a number of through-holes;

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a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

27. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external pump pad electrically connected through said common wiring layer to said at least two chip electrodes.

28. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of working formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship

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with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

29. (Amended) A semiconductor device comprising:

a wiring substrate having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said wiring substrate and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

33. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

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said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

34. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

35. (Amended) A semiconductor device comprising:

a TAB (tape automated bonding) tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on the other surface of said TAB tape and having at

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least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

said TAB tape having a number of through-holes;

a number of bumps formed respectively in said through-holes in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

39. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged from an edge of said semiconductor chip toward its inner side;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

40. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

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a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring is bent at at least one position;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

41. (Amended) A semiconductor device comprising:

a TAB tape having a predetermined pattern of wiring formed on one surface;

a semiconductor chip disposed on said one surface of said TAB tape and having at least one chip electrode set comprising at least two chip electrodes in a common wiring layer, wherein said chip electrodes are arranged parallel to an edge of said semiconductor chip and said wiring has an end width larger than an inter-electrode distance between said chip electrodes;

a number of bumps disposed on said wiring respectively in conforming relationship with said at least two chip electrodes and electrically connecting said wiring with said at least two chip electrodes; and

an external bump pad electrically connected through said common wiring layer to said at least two chip electrodes.

Please add new claims 45-56 to read as follows:

--45. A semiconductor device according to claim 21, and comprising at least two chip

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electrode sets each comprising at least two chip electrodes in a common wiring layer.

46. A semiconductor device according to claim 22, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

47. A semiconductor device according to claim 23, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

48. A semiconductor device according to claim 27, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

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49. A semiconductor device according to claim 28, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

50. A semiconductor device according to claim 29, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

51. A semiconductor device according to claim 33, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

52. A semiconductor device according to claim 34, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

53. A semiconductor device according to claim 35, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

54. A semiconductor device according to claim 39, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

55. A semiconductor device according to claim 40, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.

56. A semiconductor device according to claim 41, and comprising at least two chip electrode sets each comprising at least two chip electrodes in a common wiring layer.--

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